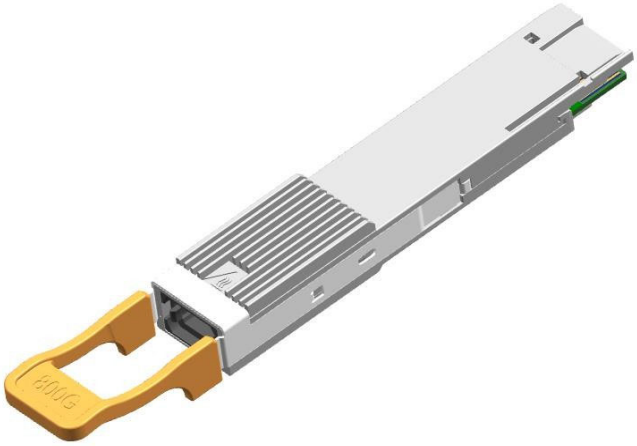
Specification

Quad Small Form-factor Pluggable Double Density
Optical Transceiver Module
QSFP-DD 400GBASE-DR4
(Preliminary)



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Ordering Information:

Model Name	TQS–R16B9–CCZ	Note
Voltage	3.3V	
Device type	850nm VCSEL	
Temperature	0°C~+70°C	
Distance	500m (SMF)	
Optical interface	MPO16 connector	
Latch Color	Beige	

Features

- Hot-pluggable QSFP-DD form factor
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- Up to 500m on SMF with FEC
- MPO-12 APC connector
- Case operating temperature: 0 ~ +70°C
- Power dissipation: < 10.5W
- Single 3.3V power supply voltage
- Compliant to CMIS 5.2
- Compliant to IEEE 802.3bs
- RoHS Compliant

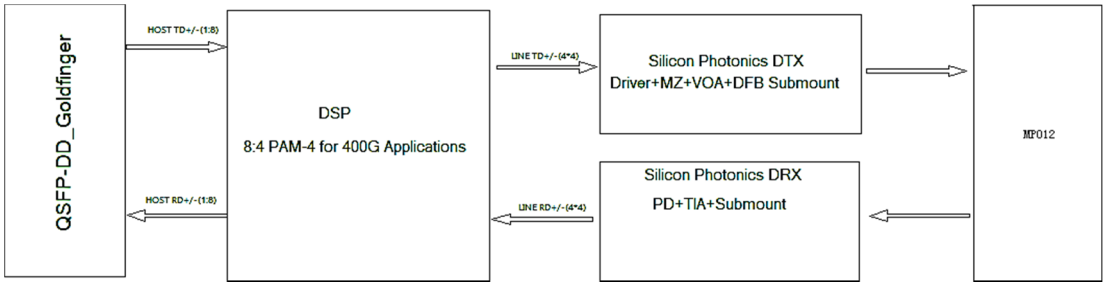
Applications

- 400G Ethernet
- Data Center
- InfiniBand interconnects

General Description

TQS-R16B9-CCZ is a Silicon Photonics 400G (4x100G) DR4 transceiver. TQS-R16B9-CCZ is a fully integrated, 425 Gb/s optical transceiver for SMF links up to 500m. TQS-R16B9-CCZ transmits data in compliance with the optical interface specification IEEE Std802.3-2018 Section 8 400GBASE-DR4. 400GBASE-DR4 specifies the use of 4-level pulse amplitude modulation (PAM4) at 53.125 Gbaud operating at four parallel channels with wavelength on the range of 1304.5-1317.5nm. The bit rate per lane is 106.25 Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO-12 connector ports to PIN-PD built in PIC (Photonic Integrated Circuit) to recover the PAM4 for interfacing with the electrical interface via with transimpedance amplifier (TIA) surfaced-mounted to PIC.

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	0		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity (no-condensation)	RH	-		85	%	
Case Operating Temperature	Tc	0		70	℃	
Receiver Damage Threshold, per Lane	PRdmg	-		+5	dBm	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an Optical input signal having this average power level.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	Vcc	3.135		3.465	V	
Supply Current per end	Icc			3182	mA	
Total Power Consumption				10.5	W	
Operating Case Temperature	TC	0		70	℃	
Relative Humidity (non-condensation)	RH	5		85	%	
Bit Rate	BR	-		425	Gbps	

Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Signaling rate, each lane	DR		53.125		GBd	
Modulation format			PAM4			
Center Wavelength	λ	1304.5	1310	1317.5	nm	
Side-mode suppression ration	SMSR	30			dB	
Average launch power, each lane	P_{AVG}	-2.9		4.0	dBm	
Optical Power OMA, each Lane, max	P_{OMA}	-0.8		4.2	dBm	
Launch power in OMA outer minus TDECQ		-2.2			dBm	
Transmitter and dispersion eye closure (TEDCQ), each lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
Optical Return Loss Tolerance	TOL			21.4	dB	
Optical Power for TX DISABLE	P_{OFF}			-15	dBm	
Receiver						
Data rate per lane	BR		53.125		GBd	
Modulation format			PAM4			
Center Wavelength	λ	1304.5	1310	1317.5	nm	
Damage Threshold, average optical power, each lane	THd	5	-	-	dBm	
Average receive power, each lane		-5.9	-	4.0	dBm	1
Receiver Reflectance	Rr		-	-26	dB	
Receiver sensitivity, each lane	SEN		Max (-3.9, SECQ - 5.3)		dBm	
Stressed receiver sensitivity, each lane	SRS			-1.9	dBm	
RX LOS Assert	LOSA	-15		-7.9	dBm	
RX LOS De-assert	LOSD			-7.4	dBm	
RX LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

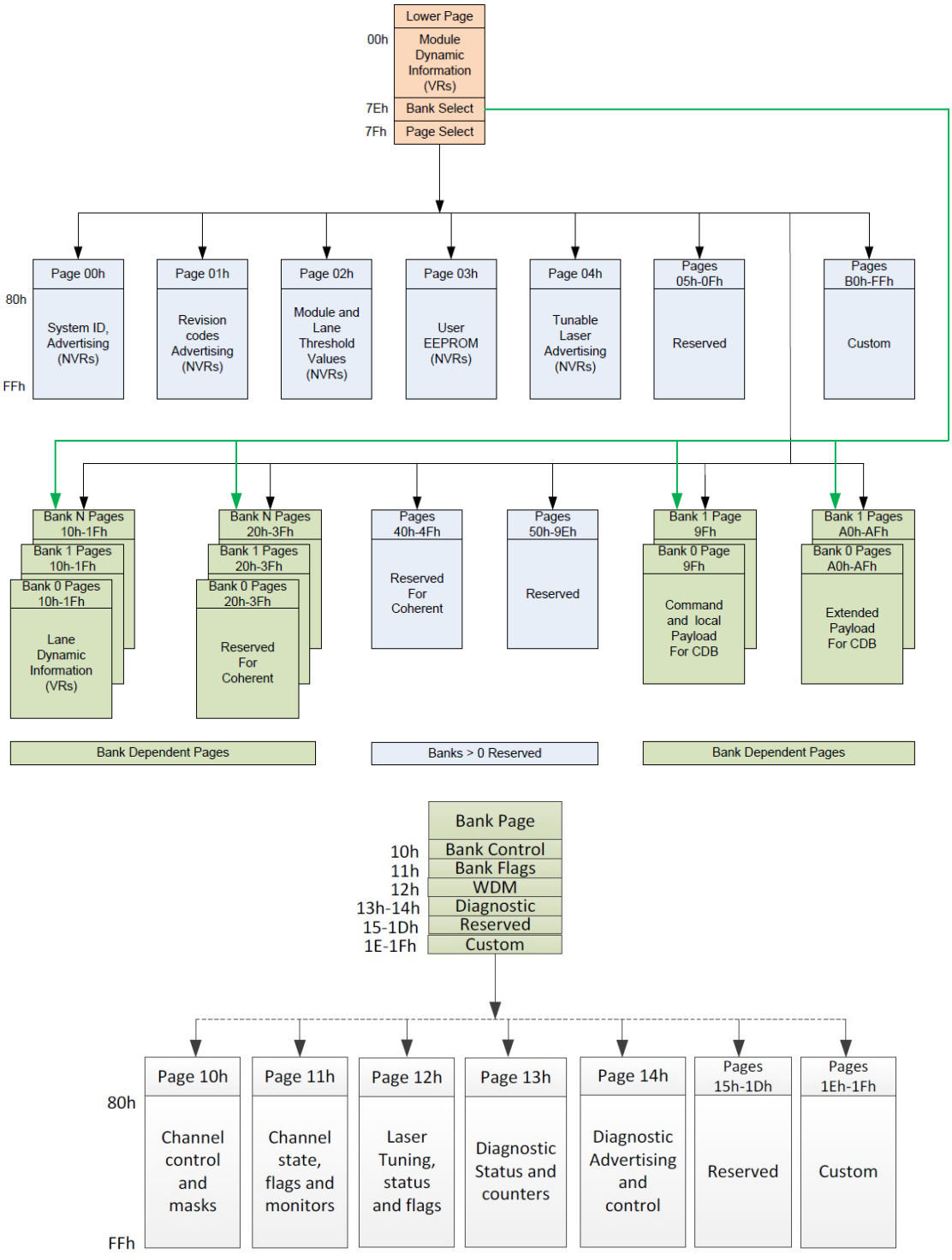
Electrical Characteristics

Parameter	Min	Typ.	Max	Unit	Note
Supply Voltage	3.135		3.465	V	
Input Differential Impedance	90	100	110	Ω	
Differential data input swing			880	mVpp	
Differential data output swing			900	mVpp	
Bit Error Rate			2.4E-4		
Input Logic Level High	2		Vcc		
Input Logic Level Low	0		0.8	C	
Output Logic Level High	V_{cc} - 0.5		Vcc	V	
Output Logic Level Low	0		0.4	V	

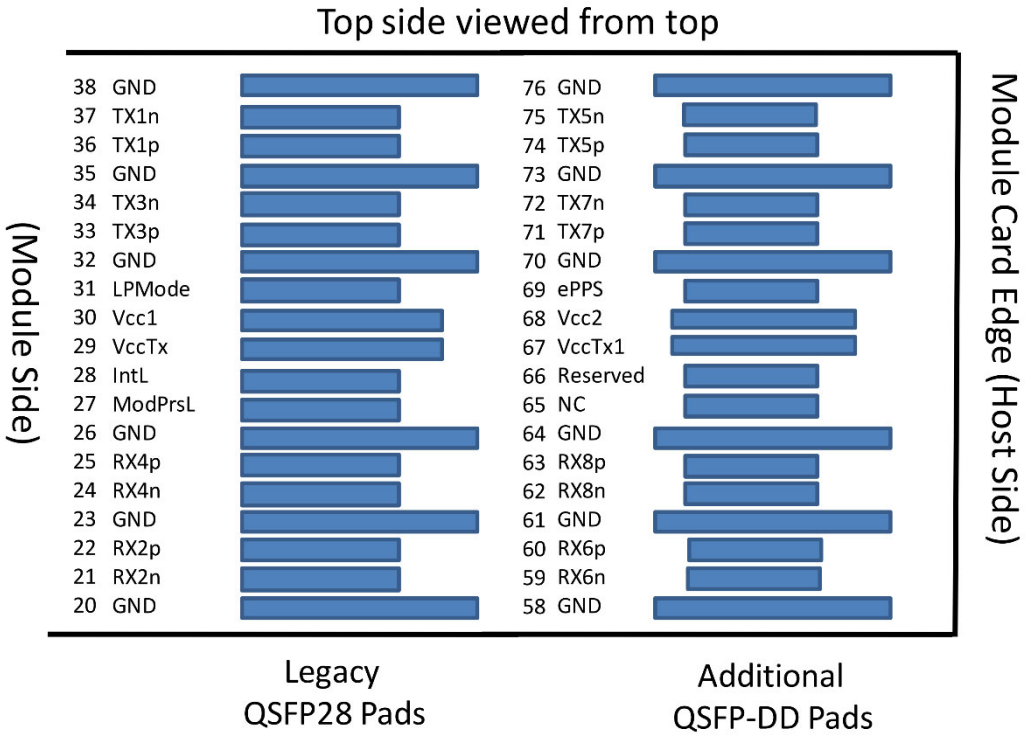
Digital Diagnostic Monitor Accuracy

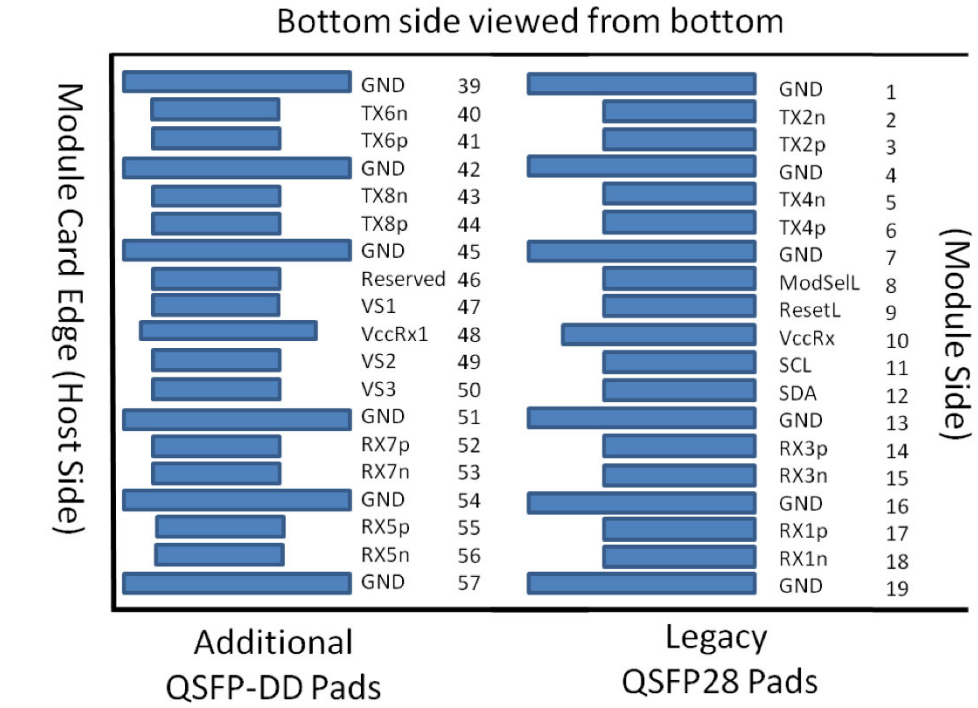
Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+ /-3	^{O}C
Internally Measured Transceiver Supply Voltage	+ /-3	%
Measured Tx Bias Current	+ /-10	%
Measured Tx Output Power	+ /-3	dB
Measured Rx Receiver Average Optical Power	+ /-3	dB

CMIS Memory Map



QSFP-DD Module Pad Assignments and Descriptions





Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	

35		Ground	GND	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		Ground	GND	1B	1
39		Ground	GND	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	
42		Ground	GND	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		Ground	GND	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific2	3A	3
50		VS3	Module Vendor Specific3	3A	3
51		Ground	GND	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		Ground	GND	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		Ground	GND	1A	1
58		Ground	GND	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		Ground	GND	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		Ground	GND	1A	1
65		NC	No Connect	3A	3
66		Reseved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		Ground	GND	1A	1

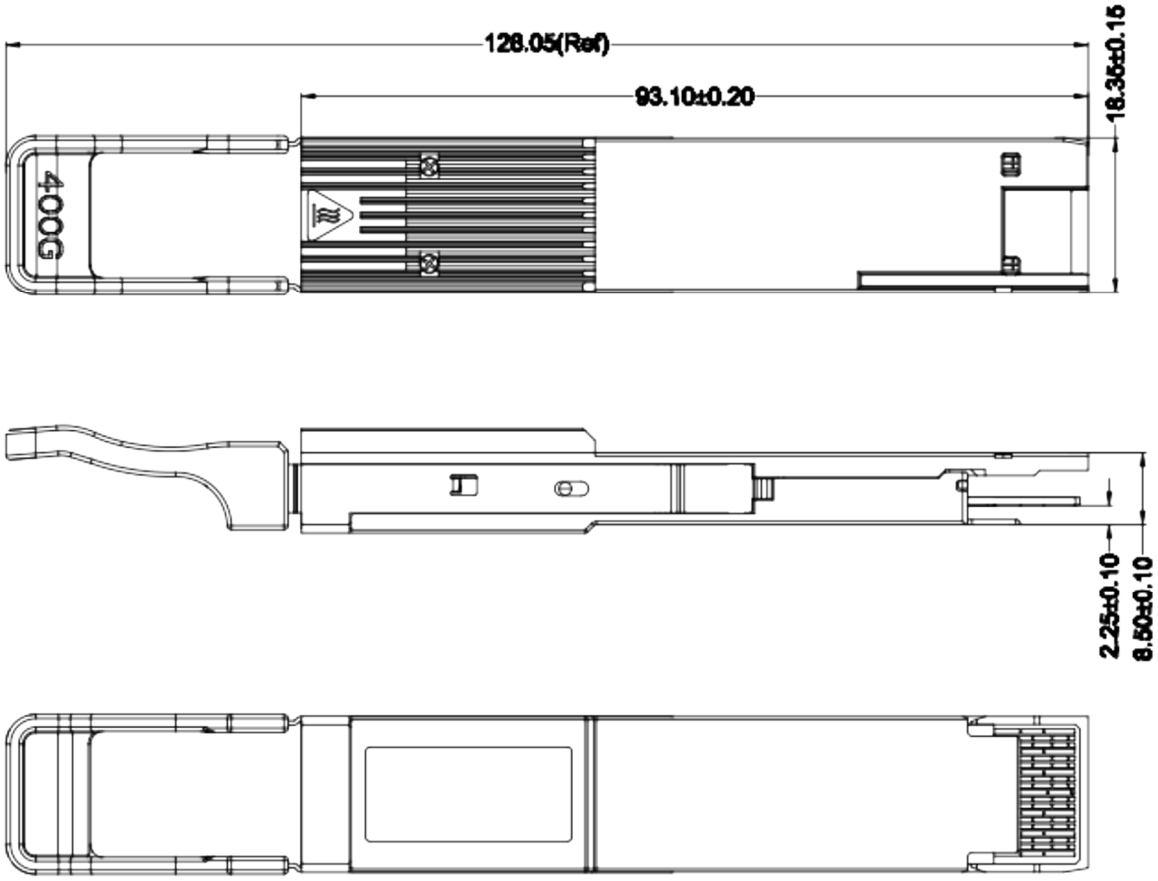
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		Ground	GND	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76	CML-I	Ground	GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Mechanical Design Diagram

(Unit: mm)



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Revision History

Date	Version	Description
5/22/2024	0.1	Preliminary release